

# **An 8192-Channel Grating Light Valve for Ultra- Violet Direct-Write Lithography**

## Introduction

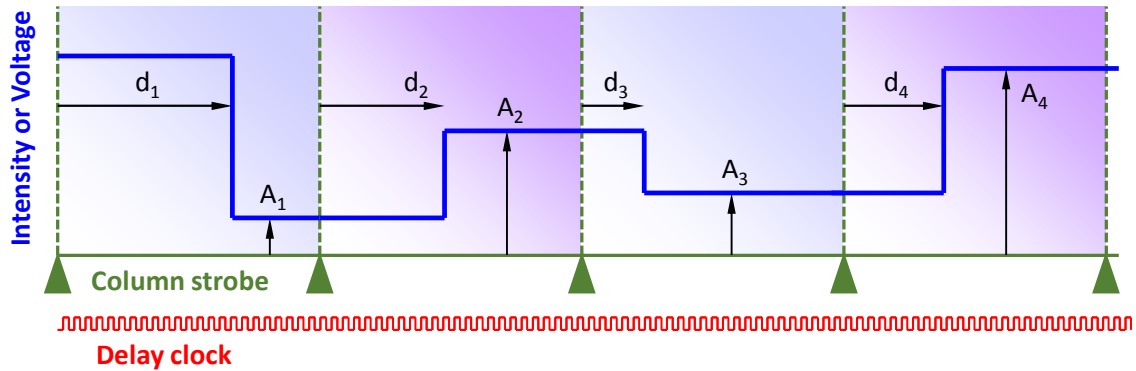
Silicon Light Machines has developed a new 8192-channel spatial light modulator for ultra-violet direct imaging (“UVDI”). Based on Grating Light Valve™ (GLV) technology, the modulator provides high-resolution control of laser intensity and edge timing at operating wavelengths ranging from 350-410nm. Analog intensity control is supported through 10-bit amplitude levels, and edge timing control is supported by 8-bit digital delay. The module supports variable line-refresh rates between 50 and 250 kHz. By combining the high intrinsic speed of the Grating Light Valve together with precise amplitude and delay control electronics, a module with unparalleled capability has been realized. This enables control of printed features at sub-grid resolutions well below the minimum printed feature size, effectively delivering higher resolution without compromising throughput. Used in conjunction with line-shaped illumination, the module has been field qualified for 10,000 hour lifetime at peak power densities of up to 3200W/cm<sup>2</sup>.



**Figure 1. 8192-Channel Ultra-Violet Direct Imaging (UVDI) module**

Parameter	Value	Units
Pixel count	8192	pixels
Operating wavelength	350-410	nm
Optical efficiency (0-order)	80	%
Contrast ratio (0-order)	300	-
Amplitude resolution	10	bits
Delay resolution	8	bits
Optical rise & fall time	< 200	ns
Optical damping time	800	ns
Column refresh rate	50 - 250	kHz
Data rate	12.7	Gbps
Power dissipation	45	W
Peak power density	3200	W/cm <sup>2</sup>

**Table 1. Principal specifications for 8192-channel UVDI module**



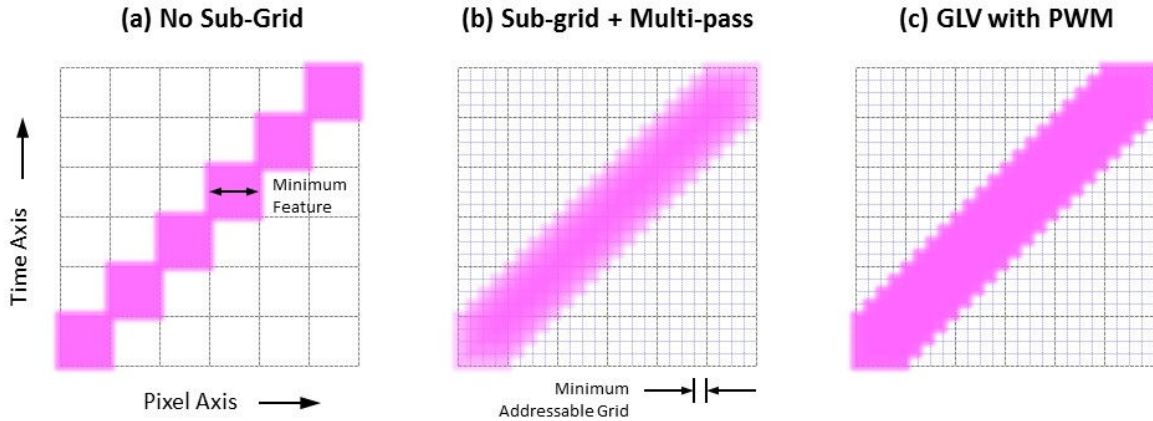
**Figure 2: Schematic of amplitude & delay functionality of UVDI modulator. Each channel supports programmable 10-bit analog amplitude ( $A_i$ ) and 8-bit digital delay ( $D_i$ ), controlled by system inputs column strobe pcs and delay clock wclk.**

Figure 2 schematically illustrates the amplitude and timing control embodied in each pixel of the UVDI modulator. The blue line can represent either drive voltage or optical intensity. External timing inputs are column strobe (pcs) and delay clock (wclk). These signals are generated on the lithography tool and represent the physical speed of the stage. Column strobe pcs divides elapsed time into discrete time periods or columns. A typical column period is 4 $\mu$ s (250 kHz). Delay clock wclk is a higher-frequency signal used in conjunction with the programmable delay function to provide fine control of control of transition timing.

As shown in Figure 2, a single optical transition can occur within one column period (provided the amplitude value changes between columns). An 8-bit digital delay value instructs when the amplitude update occurs within the column period. A digital counter in each channel counts elapsed wclk cycles since the last column strobe. A comparator in each channel compares this against a programmed digital delay value (0-255) and executes the amplitude update when a match is detected. For maximum resolution, the wclk period would be  $1/(2^8)=1/256$  of the column period. In practice, the number of wclk periods is typically set to a lower value such as 200-240. Unique amplitude and delay values can be updated for all pixels independently and at every column period.

But what is the utility of a programmable delay function? Most high-throughput direct-write lithography systems operate with continuous media motion (as opposed to step and expose mode). In continuous print systems, a high speed modulator equipped with programmable delay can be used to achieve superior resolution as illustrated in Figure 3. Figure 3a shows a minimum feature printed on a grid pitch of the same dimension. In this case, some features (such as the diagonal line shown) are not represented with sufficient resolution. In continuous print systems using 2D spatial light modulators, this can be ameliorated in by re-exposing the minimum feature at a sub-grid resolution finer than the minimum feature (1/4 sub-grid shown in 3b). However, while this improves resolution, it requires four times the number of individual exposures, thereby degrading throughput. Figure 3c illustrates printing scheme used with in the UVDI module. Programmable delay is used to place edges onto the sub-grid in the time axis, and the programmable amplitude of each pixel is used to place edges onto the sub-grid of the orthogonal (pixel) axis. This allows the UVDI module to achieve sub-grid resolution in a single pass. Note that the number of pixels assigned to a minimum feature is completely variable. Depending on contrast and resolution requirement, one, two, three or more contiguous GLV pixels can be ganged to define the minimum feature. Since the

minimum feature is not tied to the structure of the GLV, it can be displaced arbitrarily at the resolution of the GLV pixel pitch.



**Figure 3: Linear printing with spatial light modulator. (a) Minimum features printed without sub-grid delivers insufficient resolution for some patterns. (b) Re-exposing on sub-grid enhances spatial resolution, but degrades throughput. (c) UVDI uses programmable delay to achieve sub-grid resolution in a single pass.**

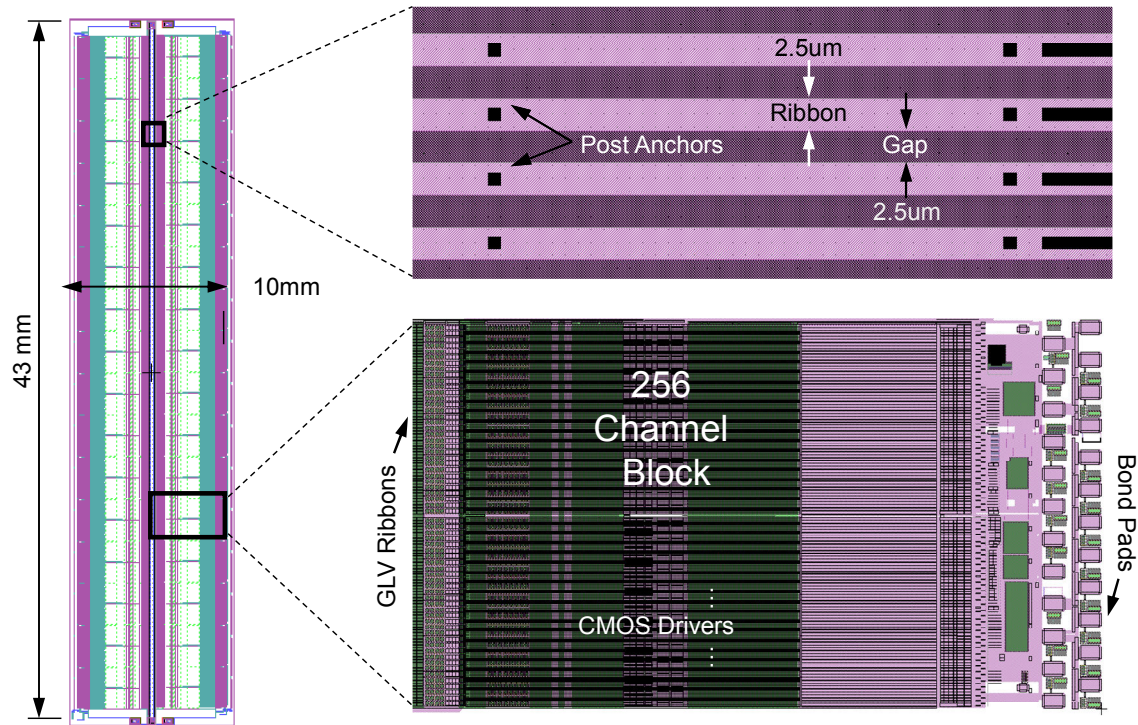
The objective of this white paper is to introduce the operating principle and capabilities of the 8192-channel GLV modulator. We begin with a description of the GLV modulator including a review of the custom hybrid CMOS/MEMS process developed to enable this technology. Next we discuss the design & operation of the CMOS channel driver associated with each pixel. We then introduce the module-level electronic hardware supporting the GLV including deserializers, field programmable gate arrays (FPGAs), digital-to-analog converters (DACs), and programmable system-on-a-chip (PSoC) microcontroller. We briefly outline the data interface and discuss module firmware. Finally, examples of optical performance are presented, including direct-write lithography results of printed images in photo-resist.

## GLV Spatial Light Modulator

The high channel-count of the 8192-channel light modulator posed a challenge in balancing pixel width against device size. Smaller pixels facilitate smaller chips which are easier to manufacture and require less de-magnification in the lithography tool, allowing smaller, lower-cost lens systems. However, smaller modulator pixels are more difficult to design, since all CMOS circuitry must fit within a narrower channel width. The UVDI device strikes a balance between these competing factors, adopting a 5 $\mu$ m pixel width for an overall chip dimension of 43 x 10mm as shown in Figure 4. To enhance uniformity, the 8192-channel modulator is broken into 32 identical blocks of 256 channels each (lower right inset of Figure 4). Each block operates as a stand-alone chip, with independent inputs signals, clocks, supply voltages and grounds. Blocks along the left side of the chip drive even-numbered pixels, and blocks on the right drive odd-numbered pixels. Although the drive channels are segmented into blocks, no such grouping occurs for the GLV MEMS array: pixels from the left- and right-hand blocks are interlaced into an unbroken array of 8192 pixels in the GLV ribbon area.



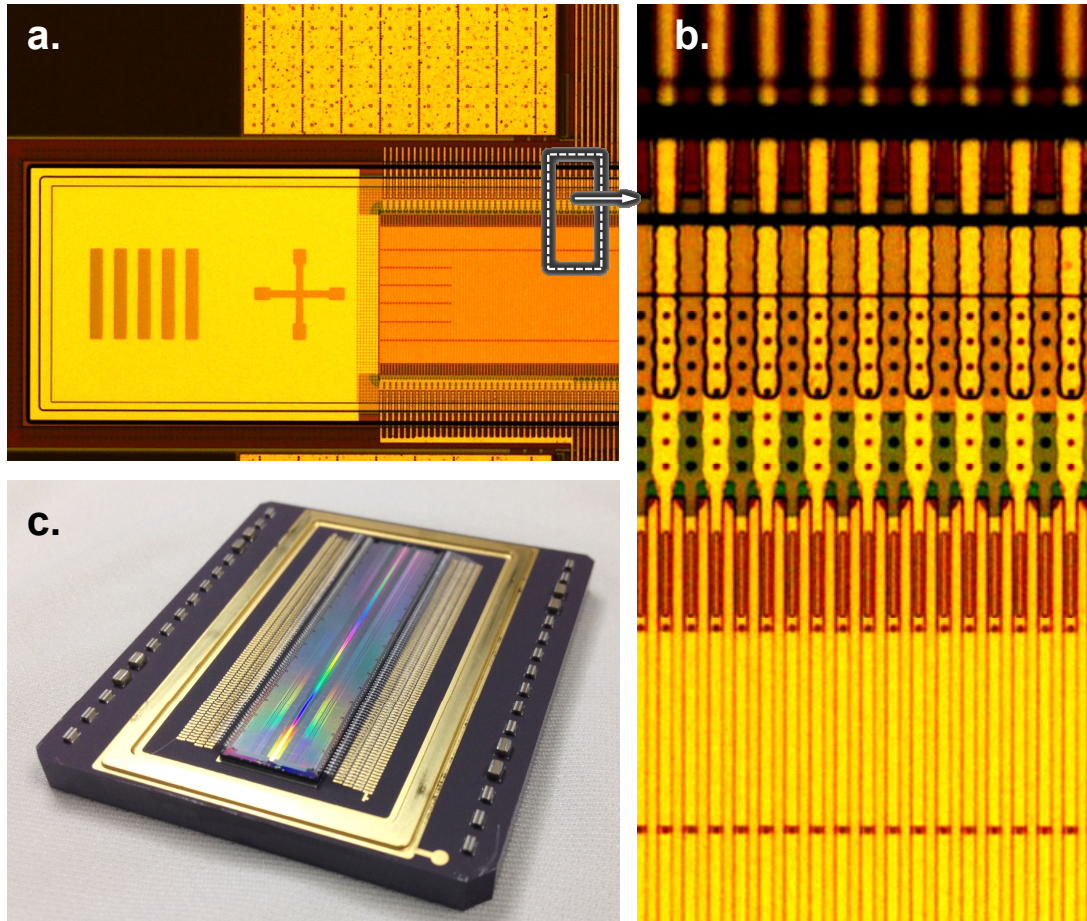
As shown in the upper right of Figure 4, each pixel is composed of one moving ribbon and one static “gap,” both 2.5 $\mu$ m wide. This design maximizes 0<sup>th</sup> order efficiency and contrast. Array reflectivity is roughly ~80% at 355nm. The ribbons are 150 $\mu$ m long and fabricated from amorphous stoichiometric LPCVD silicon nitride covered with a thin layer of sputtered aluminum which serves both as electrical conductor and optical reflector. Each ribbon is connected to the output of a dedicated CMOS driver channel.



**Figure 4: Structure of 8192-channel spatial light modulator. Each pixel comprises one ribbon and one gap each 2.5 $\mu$ m wide (upper right). GLV modulator is composed of 32 identical blocks of 256 channels each (lower right).**

Figure 5a shows a close-up of the end of the GLV ribbon array. The end bars and cross-marks are fiducial markings used for optical alignment of the GLV. Figure 5b shows a close-up of interconnect from the CMOS drivers (top) to the GLV ribbons (bottom). One set of ribbon fret posts (anchors) is visible at the bottom of the figure.

After dicing, the GLV devices are die-attached into a multi-layer ceramic package, as shown in Figure 5c. Then nearly 800 wire-bond connections are made between the perimeter die bond pads and plated lands on the surface of the ceramic substrate. These wire-bonds are barely visible along the long axis of the die in Figure 5c. The ceramic package mounts into a socket on the module. Spring loaded pins in the socket contact lands on the bottom of the ceramic substrate to establish electrical connectivity between the module and device. The package is secured in the socket by means of a Kovar window-lid. The quartz window in this lid is anti-reflection coated and angled slightly off normal to avoid glass reflections from degrading 0<sup>th</sup> order contrast.



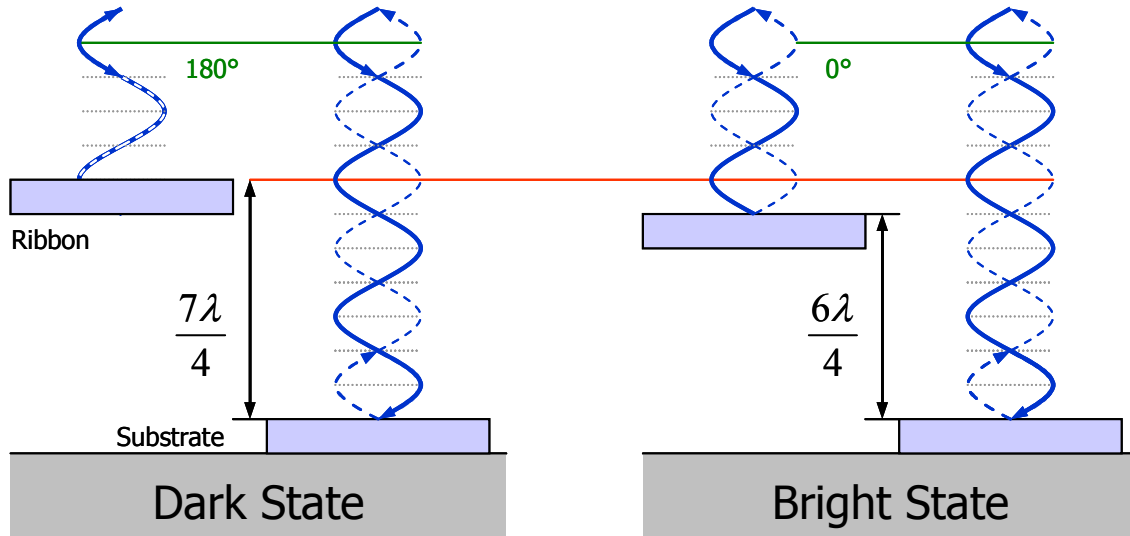
**Figure 5: 8192-channel GLV device showing (a) end of array with cross-mark alignment fiducials. (b) Detail of metal interconnect from driver channels at top to GLV ribbons at bottom. (c) Packaged device on ceramic substrate.**

Figure 6 show a cross-section through the MEMS ribbon array (along the GLV long axis, orthogonal to the GLV ribbons). The figure shows an active ribbon suspended over the substrate by a carefully controlled vertical offset. The area to the right of the ribbon represents the complementary gap region between ribbons.

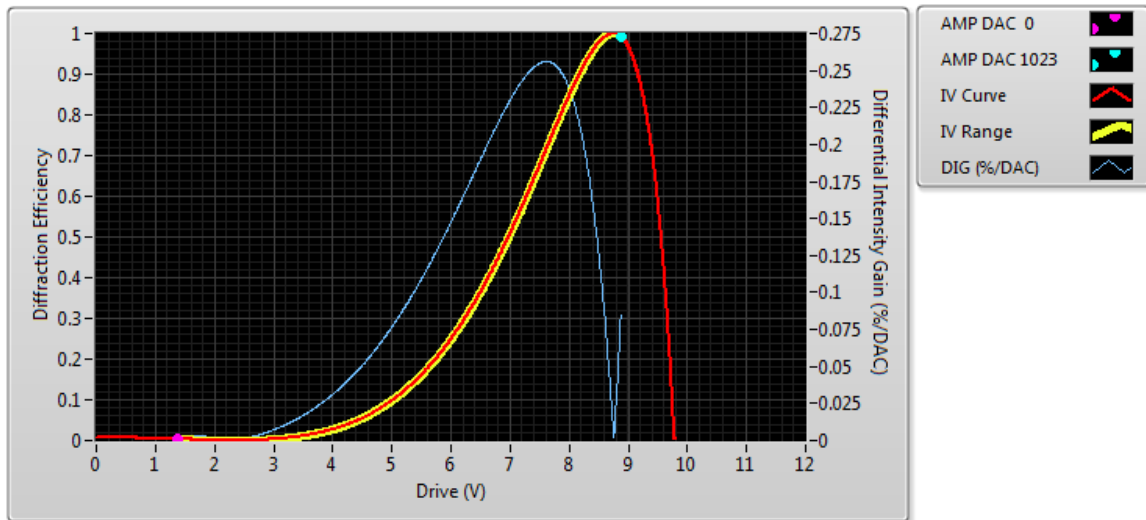
Although the GLV is fundamentally a phase modulator, contrast is generated by optical interference between light reflected from the ribbon surface and gap regions. Figure 6 (left) shows the quiescent state of the device for 355nm light. At rest, the optical path difference between the ribbon and substrate is slightly larger than  $7/4 \cdot (\lambda)$ . As such, a  $180^\circ$  phase shift is induced in the light reflected from the gap relative to light reflected from the ribbon. Destructive interference occurs and the back-reflected light (i.e. 0<sup>th</sup>-order) is suppressed. The reflected light is instead scattered into higher-order diffraction angles of the grating (i.e.  $\pm 1^{\text{st}}$ -order).

By applying an electrical potential to the ribbons (Figure 6, right), the optical path difference between the ribbon and substrate can be reduced to  $6/4 \cdot (\lambda)$  so that light reflected from the ribbon and gap regions is now in phase. Constructive interference

occurs and the 0<sup>th</sup>-order light is back reflected. By applying intermediate voltages, light can be continuously re-distributed between the 0<sup>th</sup> and  $\pm 1^{\text{st}}$ -order modes, allowing gray-scale intensity control between bright and dark states.



**Figure 6: Cross-section through GLV ribbon array. Gap thickness in quiescent state is arranged for destructive interference between light reflected from ribbon and substrate regions (dark state, left). By deflecting ribbons one quarter wavelength, constructive interference results (bright state, right).**



**Figure 7: 0<sup>th</sup>-order 355nm IV curve for UV modulator (red curve). Yellow shows the adjusted voltage range of CMOS driver. By limiting driver voltage from just below dark rollover to just above bright rollover, highest amplitude resolution is achieved. Differential curve (blue) shown by a maximum of <0.3%-per-DAC.**

Figure 7 shows the intensity-voltage (IV) curve for 355nm illumination. The red curve is the 0<sup>th</sup> order optical response. The yellow curve shows the adjusted voltage range

swept out by the channel driver. By limiting driver output voltage from just below dark rollover to just above bright rollover, highest amplitude resolution is achieved. The 8192-channel module allows a broad range of voltage adjustment, including (a) maximum drive voltage, (b) voltage swing range and (c) offset voltage, implemented by programmable control of the common plane potential (including negative voltages). The last item is valuable in preserving amplitude resolution with IV curves where the bright or dark rollover occurs at a voltage significantly different from zero (as is the case for 355nm illumination). The blue line in Figure 7 reports the differential-intensity-gain or "DIG." DIG represents the slope of the optical response, measured in %-reflectance change per amplitude DAC increment. As can be seen from the plot, the maximum DIG occurs at the inflection point of the IV-curve. The design target for this device was maximum DIG of < 0.3%-per-DAC at 355nm. As shown in Figure 7, this goal is achieved.

## CMOS/MEMS Integration: iGLV

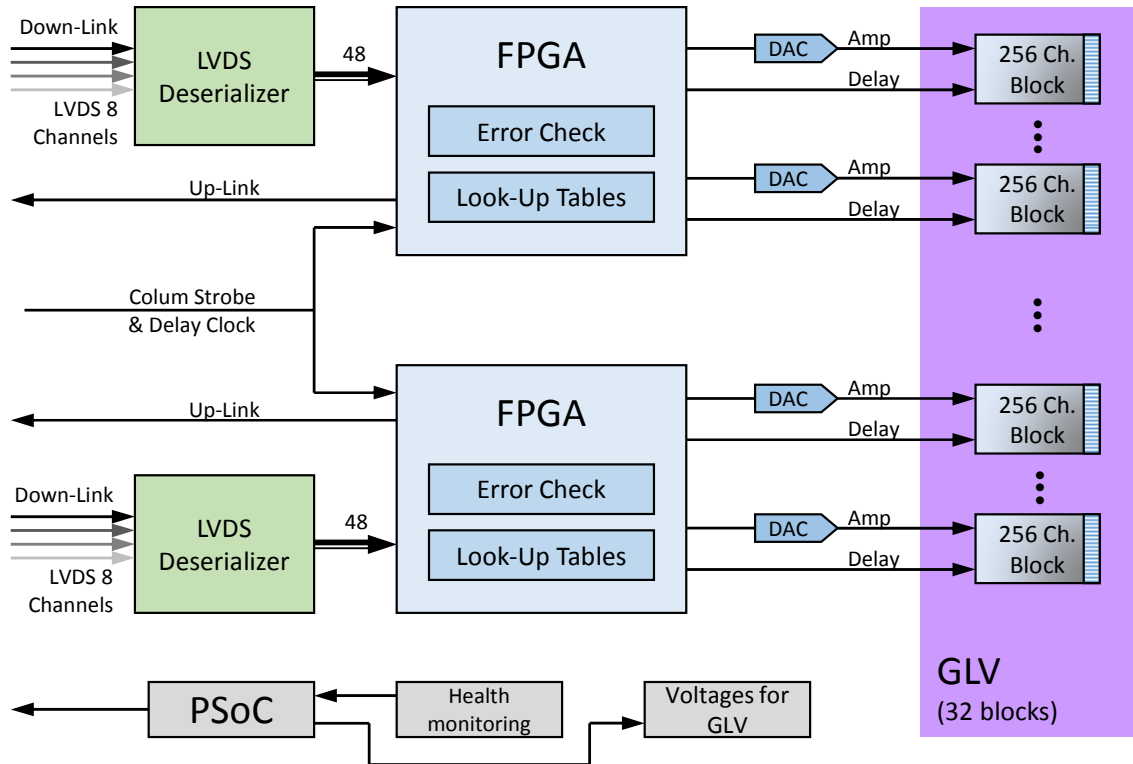
Historically, GLV modulators have been passive MEMS devices connected to CMOS drive chips by wire-bond arrays (i.e. multi-chip modules). However, for the 8192-channel device this approach was not practical due to the large area which would be required for wire-bond pads. Instead, we took the approach of integrating the CMOS driver and MEMS together on the same chip. This required merging Silicon Light Machines' GLV flow with a compatible CMOS process. We chose to integrate with the SmartMOS7 flow from Freescale Semiconductor. The resulting CMOS/MEMS hybrid process flow is called "iGLV," in which the "i" designates "integrated." The architecture of the iGLV flow is largely dictated by the thermal hierarchy of the constituent process modules. Highest temperature modules occur first, followed by successively lower temperature modules: i.e., (i) transistors, (ii) MEMS, (iii) interconnect and (iv) release. Highlights of the iGLV process are listed below.

- 0.35um CMOS with high voltage NMOS (40V)
- Three metal layers (AlCu) with refractory liners
- Titanium-nitride local interconnect for lower electrode on GLV
- Low-resistance silicided poly-silicon (3Ω/square)
- High resistance poly-silicon (6.7kΩ/square)
- Tungsten plug contacts with silicide interface
- Isolated P- and N-wells
- Poly-poly capacitors



## Module Electronics

In addition to the GLV, the UVDI module incorporates a variety of support electronics needed to configure and drive the device. A functional block diagram of the module is shown in Figure 8. The major subsystems comprising the UVDI module are: (a) low-voltage differential signalling (LVDS) deserializers, (b) field programmable gate arrays (FPGAs), (c) digital-to-analog converters (DACs), (d) programmable system-on-a-chip (PSoC) microcontroller, and (e) power supplies.



**Figure 8: Block diagram of module electronics. Major subsystems include (a) LVDS deserializers, (b) FPGAs, (c) high-speed DACs, (d) programmable system-on-a chip micro-controller (PSoC) and (e) voltage supplies for GLV.**

Starting on the left of Figure 8, communication from controller board to the GLV occurs over a “down-link” interface composed of 16 high-speed LVDS serial channels each operating at a maximum of 798 Mbps. Down-link data is received and deserialized at the module by means of two DS90CR486 National Semiconductor Channel-Link ICs. These convert the 16 high-speed LVDS serial lines into two 48-bit parallel digital buses operating at a maximum of 133 MHz. The resulting maximum data throughput for the module is 12.768 Gbps.

After deserialization, data flows into two Altera Cyclone II FPGAs which decode, error-check and buffer the data. For any given column, the image data is written to one of two pixel data registers (PDRs). This dual buffer architecture allows image data from the current column to be written to one PDR while image data from the previous column is being read from the other PDR (in Ping-Pong fashion).

While the UVDI module supports “physical” 10-bit amplitude and 8-bit delay resolutions, the bandwidth required to transmit full resolution to the module at run-time would limit the maximum column rate. Instead, the 8192-channel modulator employs “logical” values configured prior to run-time. This offers the advantage of faster column rates without compromising resolution. For example, one firmware embodiment provides seven logical 10-bit amplitudes and eight logical 8-bit delays. Each of these can be represented by a 3-bit descriptor, resulting in a 67% overall data rate savings (since  $(3+3)/(10+8) = 0.33$ ). In Figure 8, each of the two 48 bit buses from the deserializers comprises 8 channels of 6 bits each (3 amplitude bits and 3 delay bits). Back-conversion from the 3-bit amplitude & 3-bit delay data to the full 10-bit amplitude & 8-bit delay occurs in real time through “logical-to-physical” look-up-tables (LUTs) in the FPGA, before the data is sent to the GLV.

The primary outputs of the FPGAs are digital signals that (a) drive the amplitude DACs and (b) drive the 4-bit DDR delay busses. The 8192-channel module uses a single differential amplitude DAC and a single 4-bit DDR delay bus for each of the thirty-two 256-channel blocks on the GLV. In addition to these outputs, the FPGAs also support a LVDS communication output or “up-link” which allows table and register data to read from FPGAs. Up-link replies are sent in response to a coded “read” command transmitted over the down-link. In summary, the FPGAs perform a variety of manipulation and formatting operations on the data before passing it to the GLV, including:

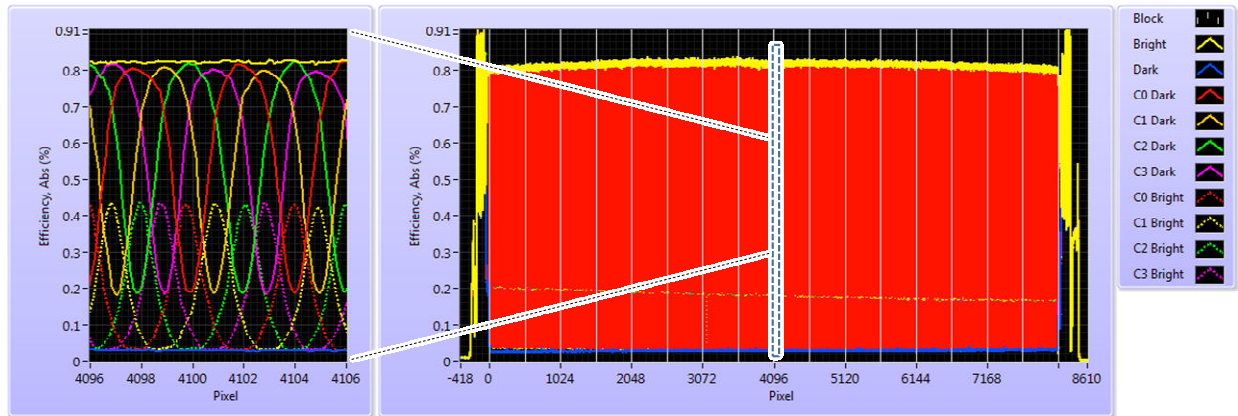
- Interfacing with LVDS deserializers
- Decoding, error checking & buffering image data
- Logical-to-physical look-up-tables for amplitude & delays
- Driving DACs for GLV amplitude path
- Driving digital delay busses for GLV delay path
- Uplink and timing interface

Finally, the 8192-channel UV modulator is also equipped with a programmable system-on-a-chip (PSoC) microcontroller for system management and health monitoring. The Cypress Semiconductor PSoC contains an 8-bit microcontroller, EEPROM non-volatile memory, programmable digital logic and programmable analog circuits. The PSoC responds to commands from the host controller board by means of an I<sup>2</sup>C communication interface and interacts with other module components (like FPGAs and temperatures sensor) by means of an SPI interface. Supported I<sup>2</sup>C commands from the controller include: (a) module power-up & power-down, (b) automatic de-skew of LVDS deserializers, (c) reset of FPGAs, (d) control of amplitude DAC operating voltage range, (e) monitoring of module voltages & currents, and (f) reading & writing to non-volatile EEPROM memory.

Power is supplied to the 8192-channel modulator by means of a single 24V input line from the controller board. All internal supply voltages (10 in total) are generated from the input source using a combination of DC-to-DC converters and linear regulators for noise suppression. Each voltage generation circuit has an enable function controlled by the PSoC for power-up and power-down sequencing. Typical current draw on the 24V supply line is 1.8A corresponding to a total power consumption of 45W.

## Optical Performance

We next present optical performance highlights from a UVDI module. Figure 9 shows a “line-scan” of a 8192-channel modulator. This plot was generated by scanning a focused CW 405nm laser along the length of the GLV array under various static ribbon configurations. The width of the scanning spot is approximately 7 $\mu$ m (full width,  $1/e^2$ ). The blue and yellow traces show the bright and dark array states respectively. Two sets of “comb” traces C1-C4 are also shown. In the comb traces, every 4<sup>th</sup> pixel is activated (either to bright or dark state) while the neighboring ribbons are held in the complementary state. This is repeated for modulo 0, 1, 2, and 3 pixels to generate the quadrature profiles shown in the inset to left in Figure 9.

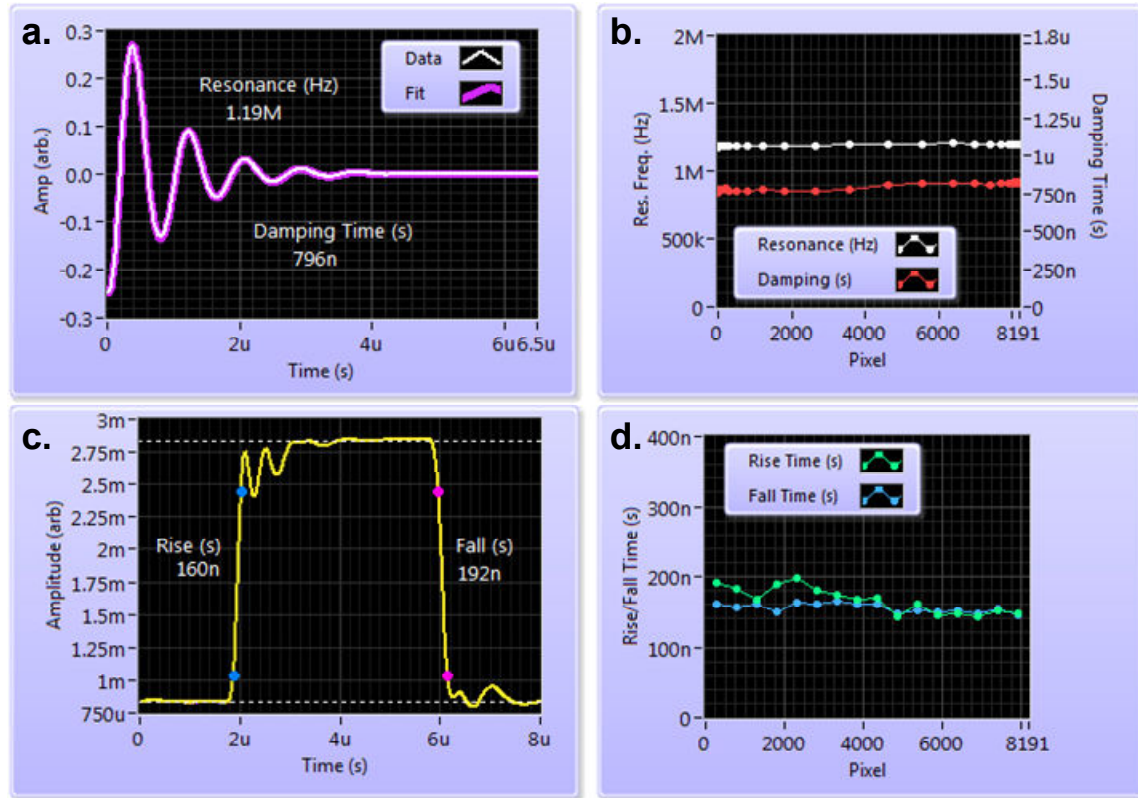


**Figure 9: Line-scan along 8192-GLV array measured at 405nm. All pixel on bright trace (yellow) and all pixel off dark trace (blue) are shown along with “comb” scans C1-C4 in which every 4<sup>th</sup> pixel is activated.**

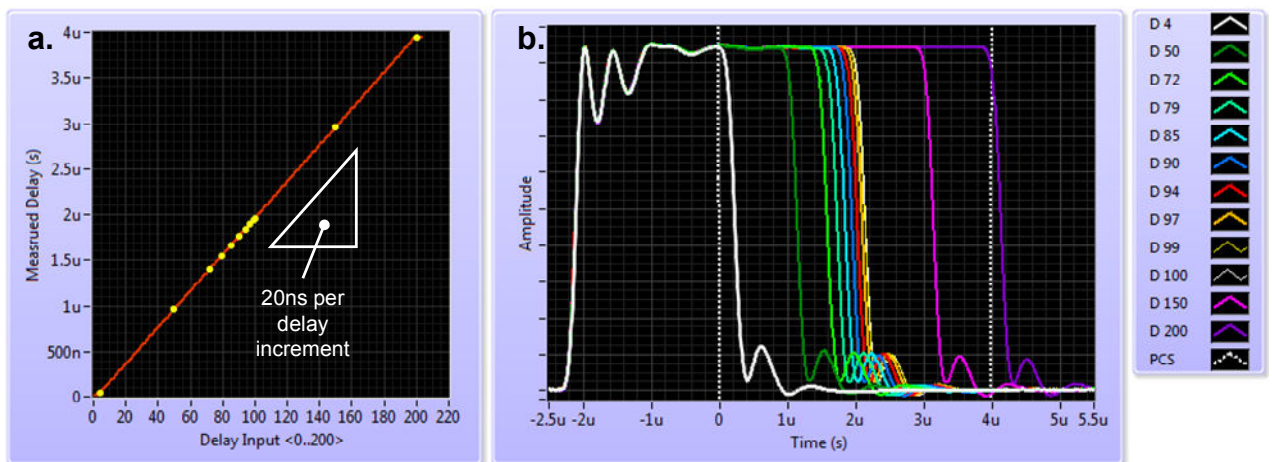
Figure 10 illustrates the dynamic properties of the GLV. Figure 10a show the optical “ring-down” curve, generated by driving a single pixel with a short voltage pulse and then allowing it to freely settle in absence of electrical drive. The ring-down curve is least-squares fit to extract the resonant frequency and damping time. Damping time refers to time required for the oscillations to reduce by a factor of  $1/e$ . Resonant frequency for the UVDI device is typically 1.2 MHz and damping time is approximately 800ns. Figure 10b shows resonance and damping as a function of position along the array. In this case the variation in resonant frequency is < 2%. Figure 10c shows a full-scale optical pulse profile (405nm). The 10%-90% rise and fall times are extracted from the pulse profile. As shown, rise/fall times are typically < 200ns for the UVDI device. Figure 10d shows rise/fall time as a function of position along the array

Figure 11 illustrates the delay capability of the UVDI module. Figure 11a shows a “delay-sweep”. The red curve was generated by sweeping the programmed delay of a single pixel from 0-200 at the minimum delay increment (20ns) and the measuring the position of the pulse edge. As shown in the plot, linearity of the delay response is excellent. Moreover, the delay is extremely uniform across the 8192 channels as a result of the digital delay architecture (delay uniformity typically < 80ns). The yellow dots in Figure 11a indicate selected delay settings illustrated in the pulse profiles shown in Figure 11b. Here we can see that the falling edge of the pulse can be programmatically

adjusted over the column period. Alternate delay settings can be used to sweep the rising edge in a similar way.



**Figure 10: (a) Free oscillation “ring-down” response of GLV ribbon. Data is fit to determine resonant frequency and damping time. (b) Plot of resonance and damping across device. (c) Full-scale bright-dark pulse used to extract 10%-90% rise and fall times. (d) Rise-fall times vs. pixel measured across device.**



**Figure 11: (a) Delay-sweep (red curve) generated by incrementing programmed delay by 20ns and measuring pulse edge position. Yellow dots indicated delay values illustrated in 13b. (b) Pulse profiles in which falling edge position is swept over the column period with arbitrary resolution.**

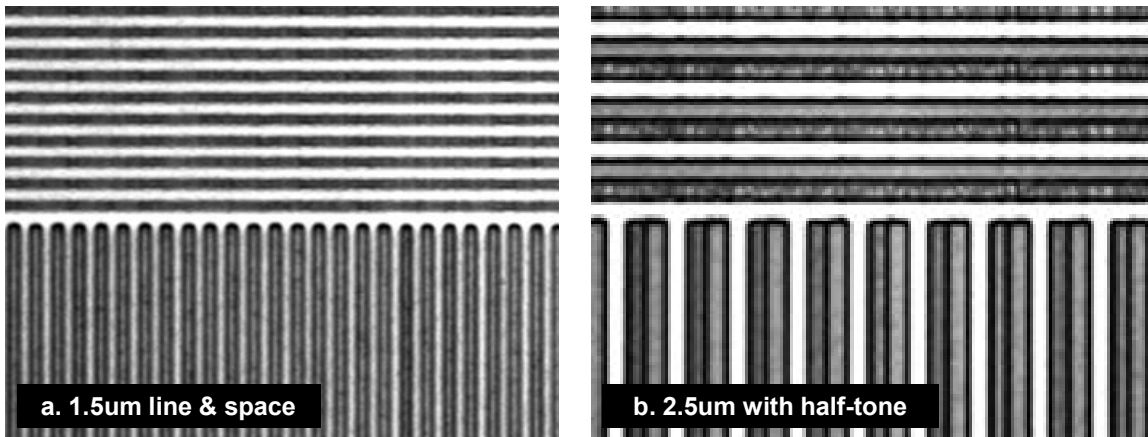


## Application to Lithography

Finally, we present direct write lithography results illustrating photo-resist images printed with the UVDI module. Recall from Figure 3c, that the print methodology employed with the UVDI module is to place a minimum feature on a sub-grid having higher resolution than the minimum feature size (MFS) itself. For example, in Figure 3c the sub-grid resolution is  $1/4^{\text{th}}$  of the minimum feature size.

Figure 12a shows 1.5  $\mu\text{m}$  vertical lines and spaces printed using 3-pixel minimum feature size at the GLV. Complementary horizontal lines and spaces were created using the programmable delay capability. By using the high resolution in edge timing, it is possible to equalize the horizontal and vertical line widths to a high degree of precision. This image was printed with 355nm illumination on i-line resist at media speed of 500mm/s using 10:1 demagnification.

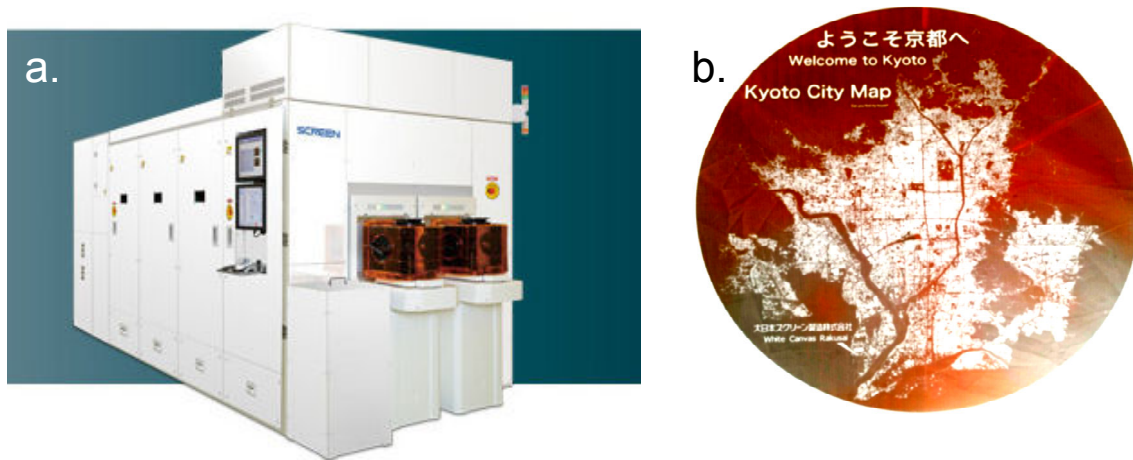
Figure 12b shows 2.5  $\mu\text{m}$  vertical lines and spaces printed using 5-pixel minimum feature size along the GLV array axis. Again, the horizontal lines were printed by using programmable delay. While Figure 12a shows binary resist image (exposed vs. non-exposed), 14b shows a tri-level printed pattern. Analog amplitude control was used to partially expose the resist, appearing as the grey region between the unexposed and fully exposed regions. The capability to “half-tone” expose resist is an area of growing interest in photo-lithography for advanced manufacturing. This analog capability sets the UVDI module apart from other spatial light modulators capable of binary exposures.



**Figure 12: Direct-write images printed with UVDI module. (a) 1.5  $\mu\text{m}$  lines and spaces using 3-pixel minimum feature size. (b) 2.5 $\mu\text{m}$  lines & spaces using a 5-pixel minimum feature. Analog gray scale used to partially expose the resist (half toning). Both images printed with 355nm illumination on i-line resist at 500mm/s with 10:1 demagnification.**

Figure 13a shows the DW3000 direct-write lithography tool produced by DNS Electronics. This tool uses two 8192-channel GLV modules and is capable of printing 200 & 300mm wafers with 3 $\mu\text{m}$  line-space resolution at throughputs of up to 65 wafers per hour. Designed for advanced packaging applications, the DW3000 allows localized control of image data to correct for warping and non-linear distortion data on a per wafer basis. Overlay capability of the DW3000 is  $\pm 1\mu\text{m}$  3-sigma. Figure 13b highlights the

direct-write capability of the tool by printing a globally non-periodic, high resolution city map of Kyoto. Under microscope inspection, individual houses and streets are visible on this map.



**Figure 13: (a) DW3000 tool from by DNS Electronics for advanced packaging direct-write lithography. Tool is capable processing 65 wafers per hour with 3 $\mu$ m line-space. (b) Global non-periodic pattern (Kyoto city map) printed onto 200mm wafer with the DW3000. Individual houses are resolved on this map.**