

# <u>RINGO - UVDI TEST BOARD</u>

## Model Number: T8192 Part Number: PWA-004285-02R

#### Features

Fully supports Aurora UVDI module evaluation and testing

Configures Aurora module parameters

Generates multiple test patterns to the module

Able to monitor Aurora module status:

- power voltages and currents
- temperature
- FPGA registers

#### Description



Ringo is a custom designed single board computer utilizing Freescale ColdFire microprocessor MCF5307. The board features a high-speed LVDS and I2C interfaces to communicate with Aurora module and RS-232 serial interface (115.2K baud rate) to communicate with a PC HyperTerminal using ASCII characters.

Power required: 3.3V DC for Ringo board and 24V DC to be provided for Aurora module. High-Speed, RS-232 and power cables are provided with Evaluation (Trial) Kit.

### **Test Patterns**

Test0 – stresses downlink data path and demonstrates the Expose Data transfer is error-free

Test1 - sets all pixels at one amplitude level with associated delay value

Test2 – toggles all pixels between 2 amplitude levels with their associated delay values

Test3 - sequences all pixels between 4 amplitude levels with their associated delay values

Test4 – sequences all pixels between 7 amplitude levels with their associated delay values

**Test5** – toggles blocks of pixels between 2 amplitude levels with their associated delay values

Test6 - modulates single pixel between 2 amplitude/delay levels and moves to the next pixel at

the "interval" time. Switching rate between 2 amplitudes is defined by last Loopcount command **Test9** – "ramps" all pixels through a series of incrementing amplitude levels. Start amplitude,

end amplitude and amplitude step size are user programmable

**Test11** – sets a block of pixels to a defined amplitude/delay level while pixels outside of the block remain at another defined amplitude/delay level

**Test12** – toggles block of pixels between 2 amplitude/delay levels while pixels outside of the block remain at one of those two amplitude/delay levels